BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

--33. (New) A device according to claim 27, wherein said second transistor further comprises a gate insulator film formed on the substrate, a polysilicon layer formed on the gate insulator film, and a side insulator film formed on a side of the gate insulator film and the polysilicon layer, said second gate electrode is formed on the polysilicon layer, and said side wall of said first gate electrode is connected to the side wall of said second gate electrode and a side wall of said side insulator film.--

REMARKS

By the present amendment, Applicants have amended claims 27, 28, 31, and 32 to more appropriately define the invention, and added new claim 33 to protect additional aspects related to the present invention.

In the Final Office Action, the Examiner rejected claims 27, 28, and 30-32 under 35 U.S.C. § 103(a) as unpatentable over Kume et al. (U.S. Patent No. 5,188,976, hereinafter "Kume"). Applicants respectfully traverse this rejection for the following reasons.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Finally, there must be a reasonable expectation of success. See M.P.E.P. § 2143. In this case, a *prima facie* case of obviousness not been established because the prior art references, taken alone or in combination, do not teach or suggest all the claim elements. More particularly, Kume does not teach or suggest at least a side wall of a

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

first gate electrode connected to a side wall of a second gate electrode as recited in claim 27.

Claims 27 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, a side wall of a first gate electrode at one end of a channel direction connected to a side wall of a second gate electrode at one end of the channel direction. In rejecting claim 27, the Examiner contends that Kume teaches a first gate electrode 21 and second gate electrode 28 are formed to be different in material and material composition. Applicants, however, respectfully submit that Kume does not teach or suggest that a side wall of a first gate electrode is connected to a side wall of a second gate electrode. In fact, Kume teaches that the first gate electrode 21 and the second gate electrode 28 are separated by a distance (Figure 11 of Kume). Therefore, Kume does not teach or suggest at least a side wall of a first gate electrode is connected to a side wall of a second gate electrode as recited in claim 27. Thus, Kume does not teach or suggest all the elements of claim 27. Since all the claim elements are not taught or suggested by Kume, a *prima facie* case of obviousness has not been established. For at least this reason, claim 27 is allowable.

Further, the Examiner cites Cronin et al (U.S. Patent No. 5,496,771 and 5,677,563, hereinafter "Cronin I" and "Cronin II" respectively) in response to the Applicants' traversal of the Examiner's assertion that damascene patterns are well-known, in the Office Action dated April 12, 2001 on page 4. In the Final Office Action, the Examiner, to support his position, alleges that Cronin I teaches damascene techniques are generally know in the art. Applicants, however, respectfully submit that neither Cronin I nor Cronin II teaches at least a side wall of a first gate electrode is

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

connected to a side wall of a second gate electrode as recited in claim 27. In fact, Cronin I and Cronin II teach that the gate electrodes of the semiconductor device are separated by a distance (Figure 4g of Cronin I and Cronin II). Therefore, Kume taken in combination with Cronin I and Cronin II would not teach or suggest the elements of claim 27. Hence, a *prima facie* case of obviousness has not been established. For at least that reason also, claim 27 is allowable.

Claims 28 and 30-32 are allowable at least due to their dependence from allowable claim 27.

Applicants have added new claim 33 to protect additional aspects related to the present invention. New claim 33 depends from patentable claim 27 and therefore incorporates all the elements of that claim. New claim 33 is patentable at least due to its dependence from patentable claim 27.

In view of the foregoing, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Attached hereto is a marked-up version of the changes made to the claims by this Amendment. The attachment is captioned "**Appendix to Amendment of March 11, 2002**".

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: March 11, 2002

By: 

Bryan S. Latham
Reg. No. 49,085

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Appendix to Amendment of March 11, 2002

IN THE CLAIMS:

Please amend claims 27, 28, 31, and 32, as follows:

27. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a first transistor formed on a first region of the substrate and including [a first insulator film and] a first gate electrode arranged along a first direction; and

a second transistor formed on a second region of the substrate and including [a second insulator film and] a second gate electrode arranged along the first direction,

wherein [said first and second insulator films are different in at least one of thickness, material and material composition, and said first and second gate electrodes are different in at least one of material and material composition] a side wall of said first gate electrode at one end of a channel direction is connected to a side wall of said second gate electrode at one end of the channel direction.

28. (Twice Amended) A device according to claim 27, wherein a part of [a] the side wall of the first gate electrode is only connected to a part of [a] the side wall of the second gate electrode and said part of the side wall of the first gate electrode and said part of the side wall of the second gate electrode are substantially perpendicular to a surface of said semiconductor substrate.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

31. (Twice Amended) A device according to claim [28] 27, wherein said first transistor includes a first insulator film, said second transistor includes a second insulator film, said first insulator film is thinner than said second insulator film, said first transistor is included in a logic circuit, and said second transistor is included in a memory cell.

32. (Twice Amended) A device according to claim [28] 27, wherein [said first and second gate electrodes are connected to each other through a connection layer and] top surfaces of said first and second gate electrodes and [said] a connection layer are coplanar.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com